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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,844	12/05/2003	En-Hsing Chen	023-0030	8322

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EXAMINER	
MAI, SON LUU	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,844	CHEN ET AL.	
	Examiner	Art Unit	
	Son L. Mai	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11,19,24-29,42,43,45,46,48-52,64,68-72,85,86 and 88* is/are rejected.

7)☒ Claim(s) *2,12-18,20-23,30-41,44,47,53-63,65-67,73-84 and 87* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09-23-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The papers filed 12-05-03, 04-05-04 and 09-23-04 have been entered. Accordingly, claims 1-88 are pending.

Information Disclosure Statement

2. The information disclosure statement filed 09-23-04 has been considered.

Drawings

3. The drawings were received on 04-05-04. These drawings are acceptable.

Specification

4. The disclosure is objected to because of the following informalities: On page 34, line 8, the reference numeral "106" should read –406--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 6-11, 24-29, 42, 45, 68-72, 85, and 88 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 6, it is not clear if the recitation "associated array lines" in line 5 is the same as "associated array lines" in line 3. An article "the" should be used for the second occurrence of the phrase if they are the same. Note that the semicolon (;) at the end of the claim should be changed to a period (.)

Claims 7-11 are rejected because in their dependency they include the limitations of based claim 6.

As for claim 24, it is not clear if the recitation "associated array lines" in line 5 is the same as "associated array lines" in line 3. An article "the" should be used for the second occurrence of the phrase if they are the same. Note that the semicolon (;) at the end of the claim should be changed to a period (.)

Claims 25-29 are rejected because in their dependency they include the limitations of based claim 24.

As for claim 42, "the memory cell switch devices" in line 1 lacks antecedent basis in the claim. Perhaps the Applicants meant "the memory cells of the memory array".

As for claim 45, "the memory cell transistors" in line 1 lacks antecedent basis in the claim. Perhaps the Applicants meant "the memory cells of the memory array".

As for claim 68, it is not clear if the recitation "associated array lines" in line 5 is the same as "associated array lines" in line 3. An article "the" should be used for the second occurrence of the phrase if they are the same. Note that the semicolon (;) at the end of the claim should be changed to a period (.)

Claims 69-72 are rejected because in their dependency they include the limitations of based claim 68.

As for claim 85, "the memory cell switch devices" in line 1 lacks antecedent basis in the claim. Perhaps the Applicants meant "the memory cells of the memory array".

As for claim 88, "the memory cell transistors" in line 1 lacks antecedent basis in the claim. Perhaps the Applicants meant "the memory cells of the memory array".

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 3-5, 19, 42-43, 45, 46, 48-52, 64, 85-86, and 88 are rejected under 35 U.S.C. 102(b) as being anticipated by Derhacobian et al. (U.S. Patent 5,991,202).

Regarding claims 1 and 46, Derhacobian et al. discloses a memory array (figure 2) including memory cells (20, 30, 40) arranged in a plurality of series-connected NAND strings (3 strings shown in figure 2), said memory cells comprising modifiable conductance switch devices (30, 40), said method comprising pulsing a selected word line (WL2) to a programming voltage (Vprog in figure 3B) a number of times to achieve an aggregate programming time for a selected memory cell, while limiting individual programming pulses to durations substantially less than the aggregate programming time, thereby limiting leakage current effects within NAND strings of a selected block (column 4, lines 11-36).

Regarding claims 3 and 48, Derhacobian et al. further teaches maintaining an inhibit voltage (Vsupp) on associated array lines (BL2) between programming pulses.

Regarding claims 4 and 49, Derhacobian et al. also teaches the leakage current effects including changes in a voltage bias at one or more locations within a NAND string that otherwise may occur during a long programming pulse. (Vpass to unselected WLs changes from 10V to 0V.)

Regarding claims 5 and 50, Derhacobian et al. teaches re-establishing a respective bias condition within selected and unselected NAND strings of a selected block before each such programming pulse (The bias condition of Vpass returns to 0V before Vprog is pulsed to 18V.)

Regarding claims 42 and 85, Derhacobian et al. discusses at column 5, lines 49-60, wherein the memory cells have more than two nominal values of conductance.

Regarding claims 43 and 86, the transistors 30 and 40 in figure 2 of Derhacobian et al. have a charge storage dielectric as every other FET transistor.

Regarding claims 45 and 88, Derhacobian et al. discloses at column 5, lines 49-60, the memory cells have a depletion mode threshold voltage of -2 volts.

Regarding claim 51, Derhacobian et al. teaches the integrated circuit of claim 46 further comprising means (transistor 30 in unselected BL2) for coupling unselected NAND strings within a selected memory block to associated array lines (at both ends of the string) conveying an inhibit voltage (Vsupp) to establish a bias condition within such unselected NAND strings.

Regarding claim 52, Derhacobian et al. discloses the integrated circuit of claim 51 wherein the array support circuitry is further configured for maintaining the inhibit voltage on the associated array lines between programming pulses. (The drain and the gate of transistor 30 of unselected BL2 are maintained at Vsupp.)

Regarding claim 64, the memory array of Derhacobian et al. comprises two-dimensional memory array having one plane of memory cells formed in a substrate (column 1, lines 13-17).

Allowable Subject Matter

9. Claims 2, 6-18, 20-23, 30-41, 44, 47, 53-67, 73-84, and 87 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 6-11, 24-29, and 68-72 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach at least the further limitations of claim 6 which calls for coupling unselected NAND strings within a selected memory block to associated array lines conveying an inhibit voltage, de-coupling unselected NAND strings within the selected memory block from the associated array lines conveying bias voltages other than the inhibit voltage.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jeong (U.S. Patent 6,614,688), Nakamura (U.S. Patent 6,108,238), Sakui (U.S. Patent 6,049,494), and Arase (U.S. Patent 5,812,457) teach circuits to alleviate programming disturbance in NAND strings cells.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

01-13-05

Son L. Mai
Primary Examiner
Art Unit 2818